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Patent
Attorney's Docket No. 024938-192

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Ronald John VANDERHELM

Application No.: 10/038,124

Filed: January 2, 2002

For: CORE WIRELESS ENGINE

Attention: **DRAFTING BRANCH**

Group Art Unit: 2681

Examiner: unknown

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SUBMISSION OF FORMAL DRAWINGS

Assistant Commissioner for Patents
Washington, D.C. 20231

ATTN: OFFICIAL DRAFTSMAN

Sir:

Enclosed please find six (6) sheet(s) of formal drawings for review by the Patent and Trademark Office in connection with the above-referenced application. Should the enclosed drawings require changes, it is respectfully requested that the Patent and Trademark Office notify the undersigned of same.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____

Joseph P. O'Malley
Registration No. 36,226
Redwood Shores, California Office
Tel: (650) 622-2333

P.O. Box 1404
Alexandria, Virginia 22313-1404

Date: February 26, 2002

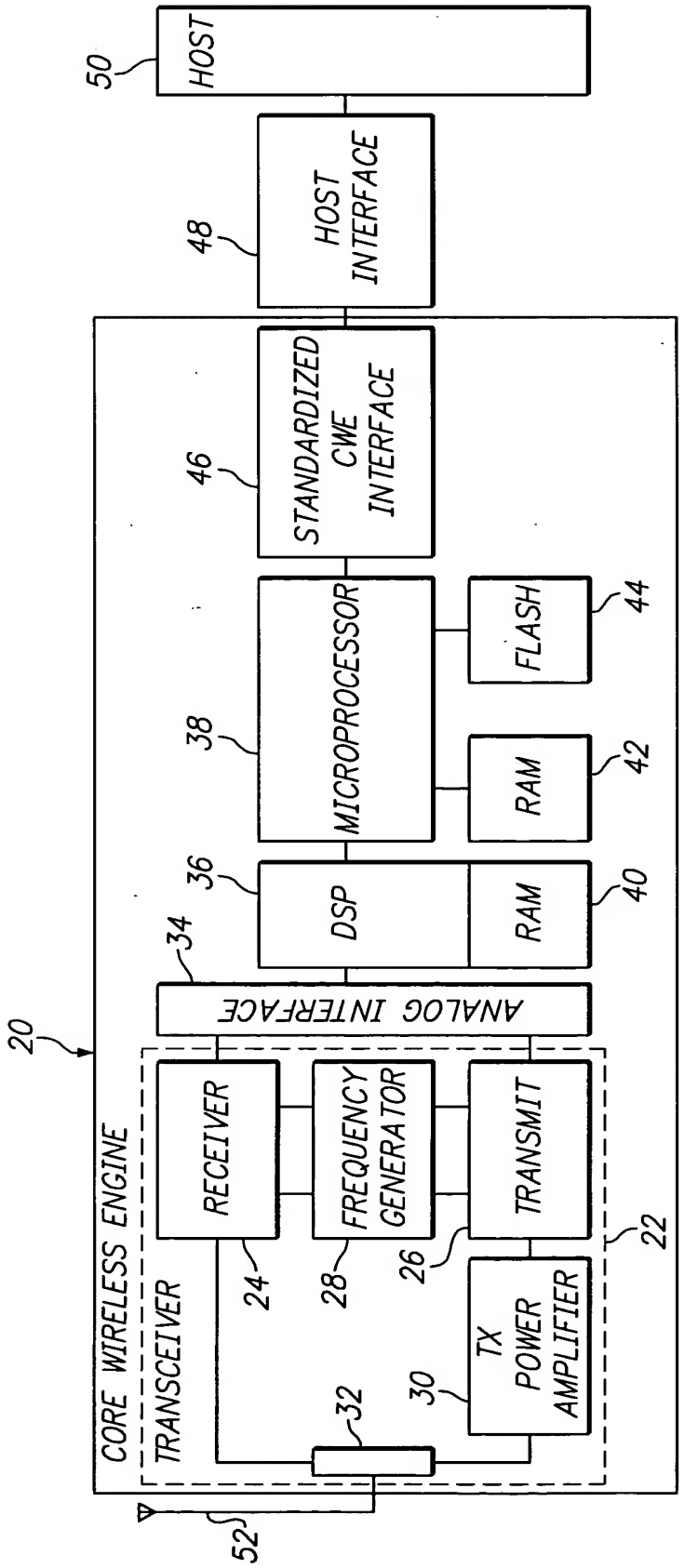

50
HOST
48
HOST INTERFACE
46
STANDARDIZED CWE INTERFACE
38
MICROPROCESSOR
FLASH
44
RAM
42
36
DSP
RAM
40
34
ANALOG INTERFACE
20
CORE WIRELESS ENGINE
TRANSCEIVER
RECEIVER
FREQUENCY GENERATOR
TRANSMIT
24
28
26
22
TX POWER AMPLIFIER
30
32
52

FIG. 1

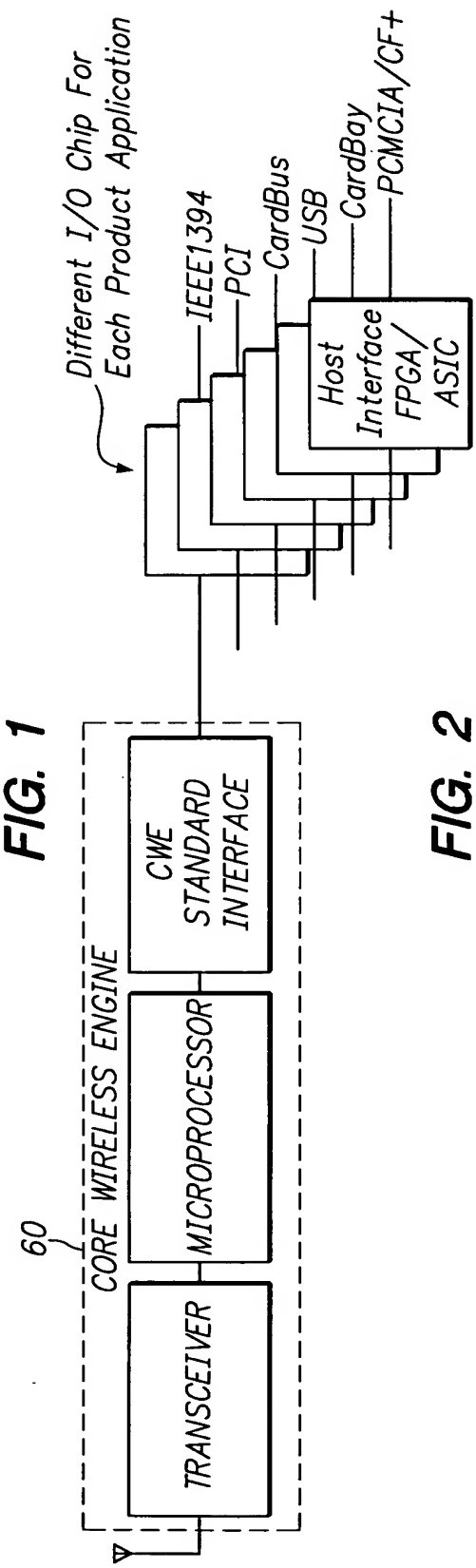

Different I/O Chip For Each Product Application
IEEE1394
PCI
CardBus
USB
CardBay
PCMCIA/CF+
Host Interface FPGA/ ASIC
60
CORE WIRELESS ENGINE
CWE STANDARD INTERFACE
MICROPROCESSOR
TRANSCEIVER

FIG. 2

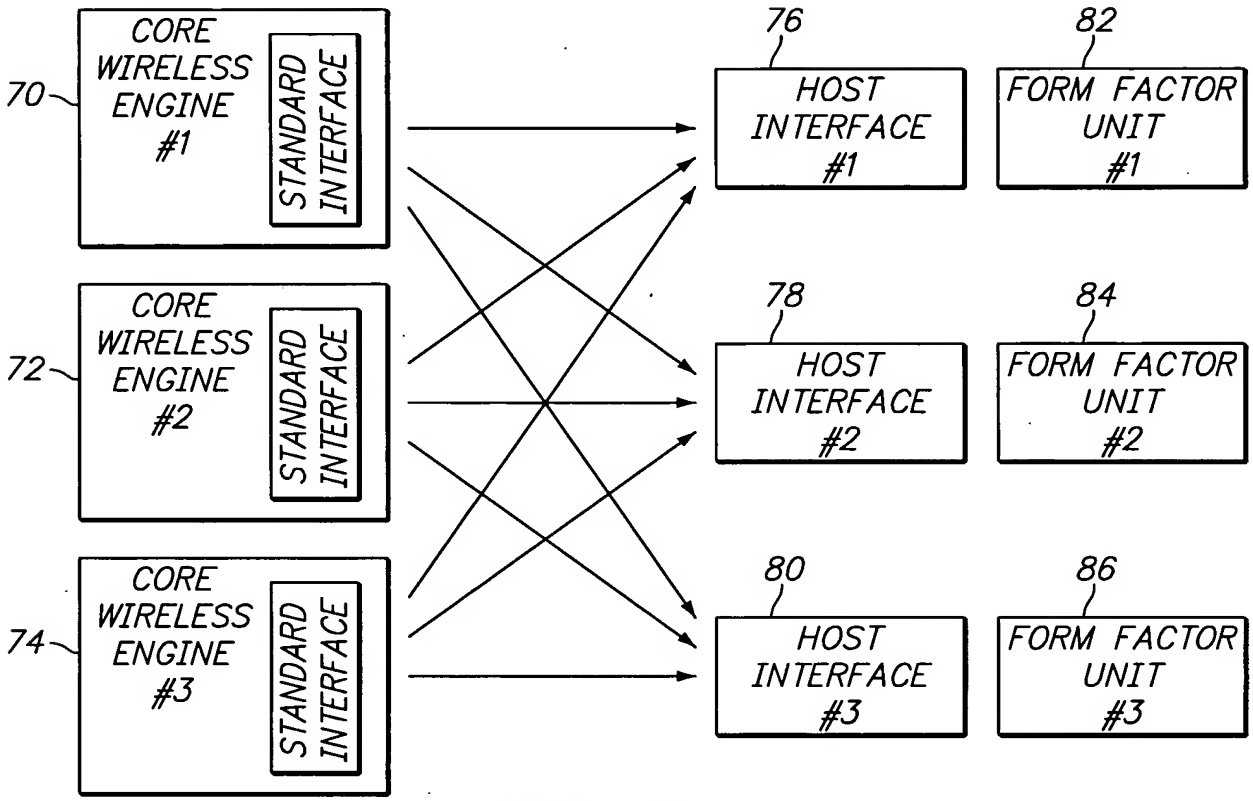

CORE WIRELESS ENGINE #1
STANDARD INTERFACE
70
CORE WIRELESS ENGINE #2
STANDARD INTERFACE
72
CORE WIRELESS ENGINE #3
STANDARD INTERFACE
74
76
HOST INTERFACE #1
82
FORM FACTOR UNIT #1
78
HOST INTERFACE #2
84
FORM FACTOR UNIT #2
80
HOST INTERFACE #3
86
FORM FACTOR UNIT #3

FIG. 3

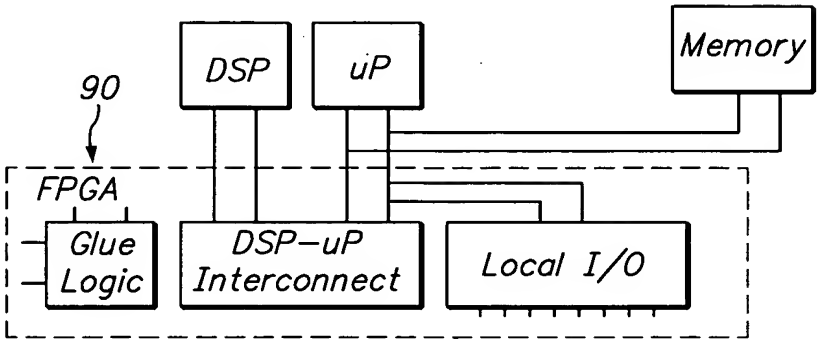

90
DSP
uP
Memory
FPGA
Glue Logic
DSP–uP Interconnect
Local I/O

FIG. 4A

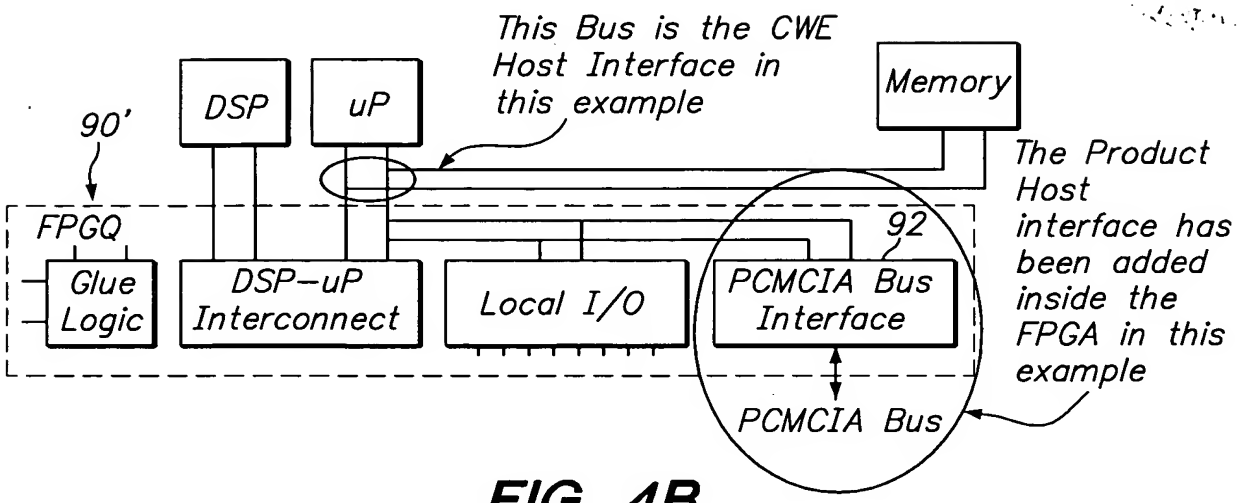

This Bus is the CWE Host Interface in this example
Memory
DSP
uP
90'
The Product Host interface has been added inside the FPGA in this example
FPGQ
92
Glue Logic
DSP–uP Interconnect
Local I/O
PCMCIA Bus Interface
PCMCIA Bus

FIG. 4B

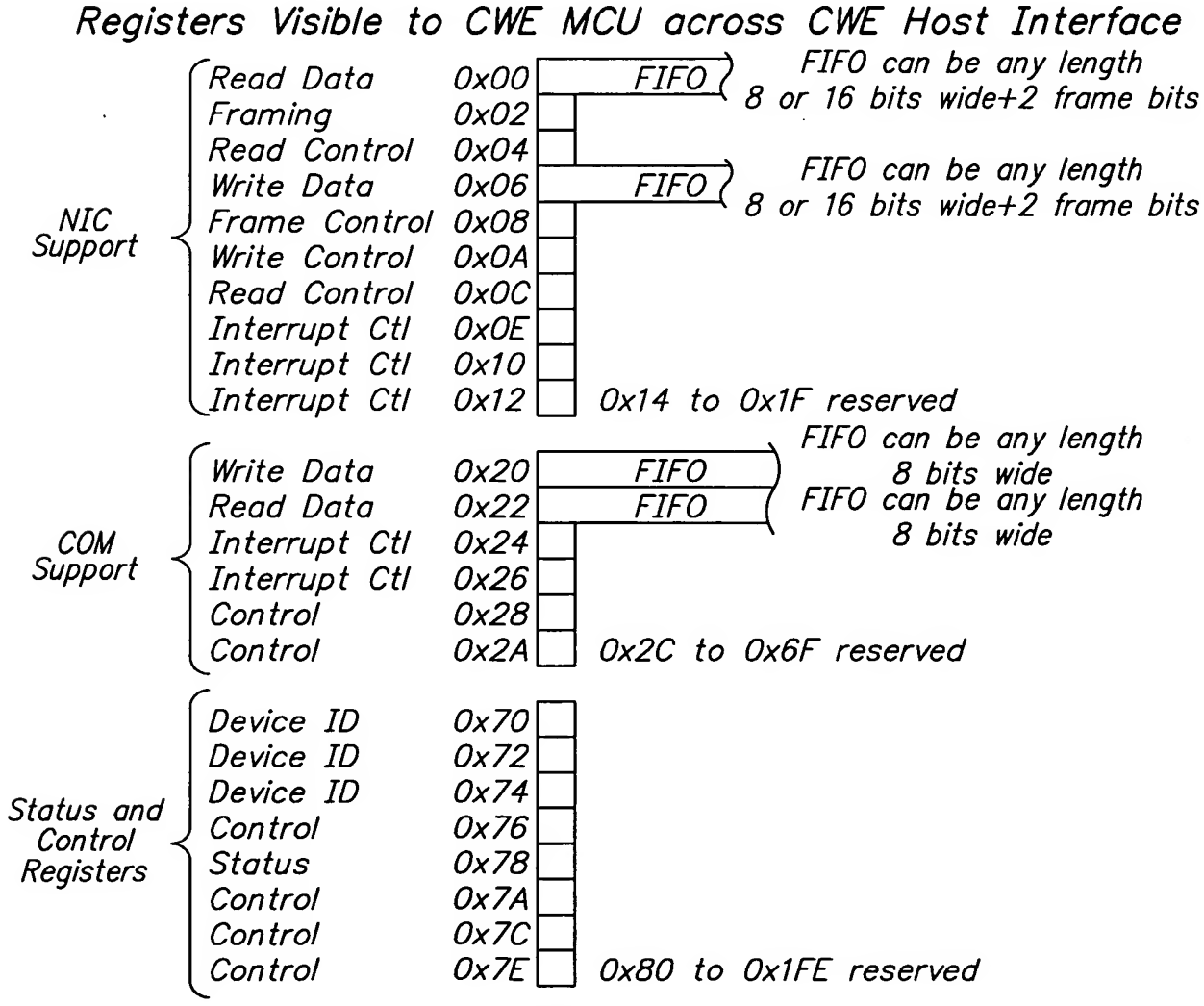

Registers Visible to CWE MCU across CWE Host Interface
NIC Support
Read Data 0x00
Framing 0x02
Read Control 0x04
Write Data 0x06
Frame Control 0x08
Write Control 0x0A
Read Control 0x0C
Interrupt Ctl 0x0E
Interrupt Ctl 0x10
Interrupt Ctl 0x12
FIFO
FIFO
FIFO can be any length 8 or 16 bits wide+2 frame bits
FIFO can be any length 8 or 16 bits wide+2 frame bits
0x14 to 0x1F reserved
COM Support
Write Data 0x20
Read Data 0x22
Interrupt Ctl 0x24
Interrupt Ctl 0x26
Control 0x28
Control 0x2A
FIFO
FIFO
FIFO can be any length 8 bits wide
FIFO can be any length 8 bits wide
0x2C to 0x6F reserved
Status and Control Registers
Device ID 0x70
Device ID 0x72
Device ID 0x74
Control 0x76
Status 0x78
Control 0x7A
Control 0x7C
Control 0x7E
0x80 to 0x1FE reserved

FIG. 5

CWE Host Interface

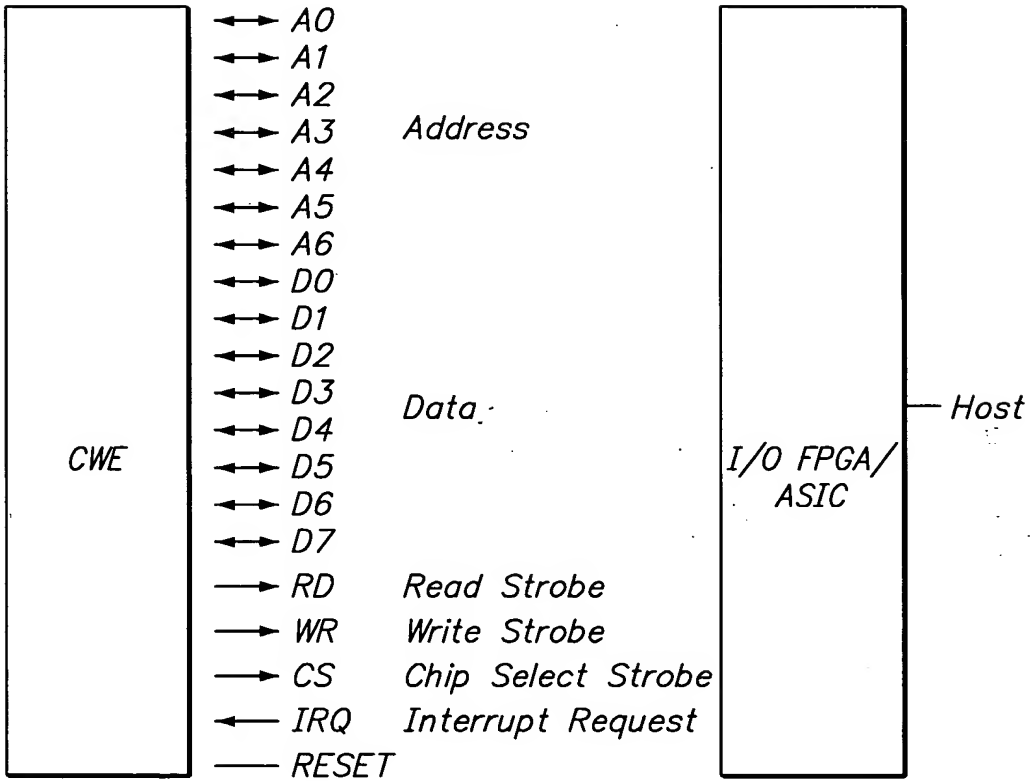


FIG. 6

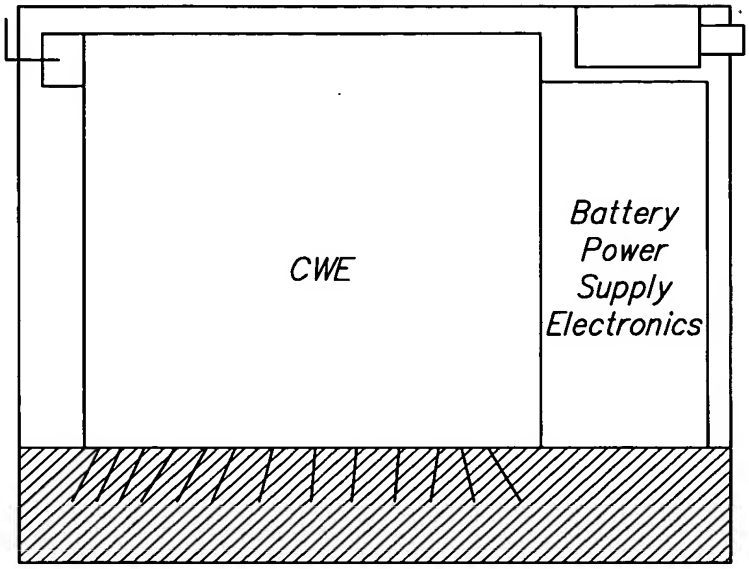


FIG. 8B

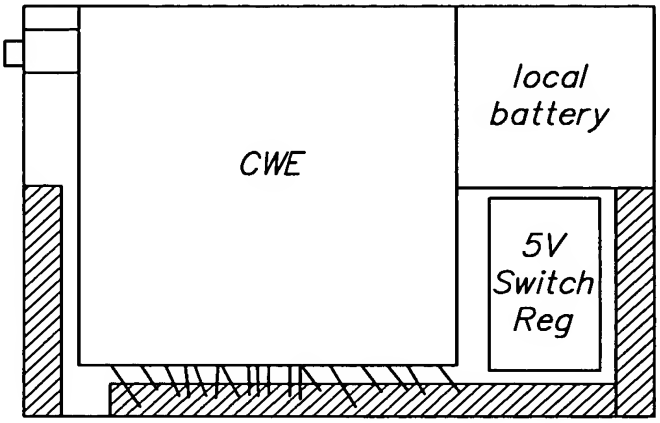


FIG. 8C

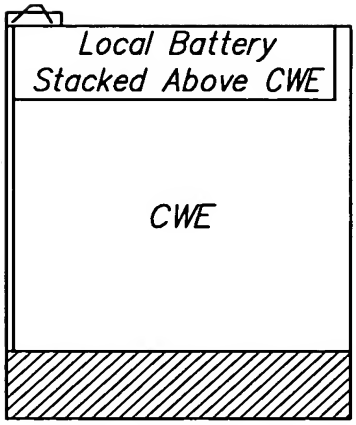


FIG. 8E

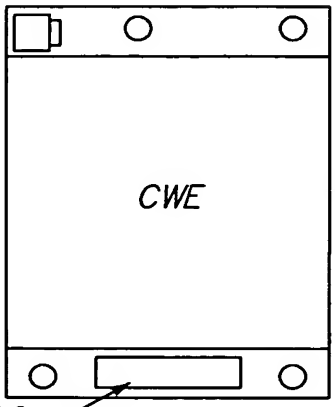
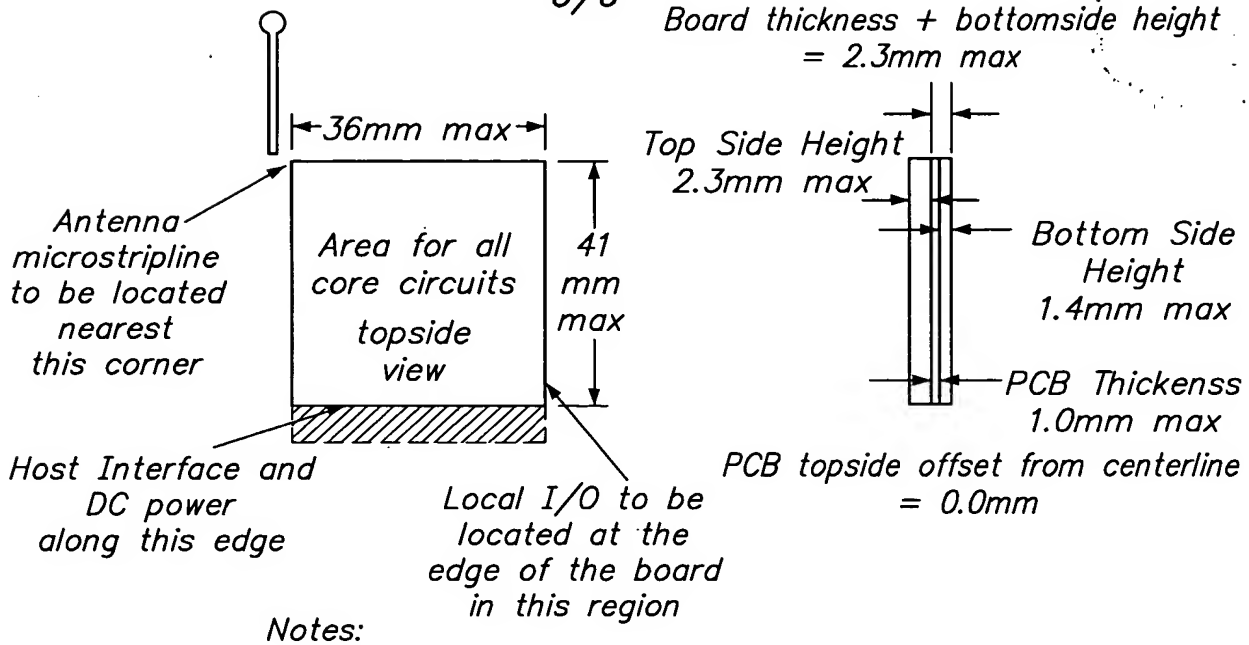


FIG. 8F



Notes:

1) RF connector and host connector fall outside the defined area, but nearest the locations shown.

2) Shielding is to be included within the dimensions shown.

3) Indicator LEDs, host connectors and other optional peripherals may be outside the dimension shown.

4) PCB Thickness at host connector will require additional buildup to 1mm when building a Mini-PCI type 3 product if core design has pcb less than 1.0mm thick

FIG. 7

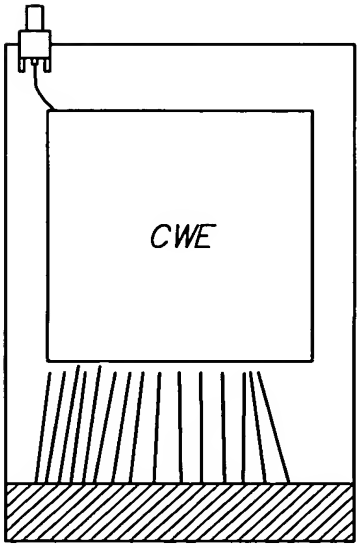


FIG. 8A

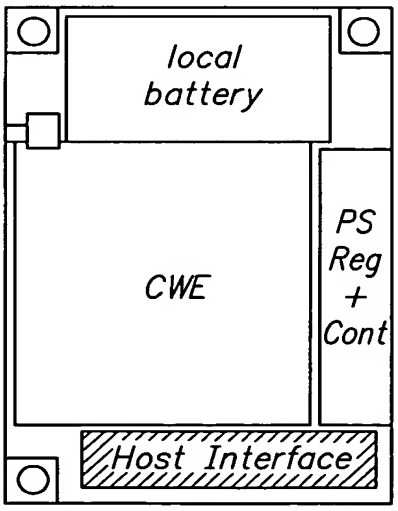


FIG. 8D